INTERNATIONAL SYMPOSIUM ON LOW POWER ELECTRONICS AND DESIGN

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JW Marriott Hotel

Seoul, Korea

ADVANCE PROGRAM

SUNDAY, August 24, 2003

18:30-20:30 Registration

MONDAY, August 25, 2003

7:00-8:45 Breakfast

8:45-9:00 Opening Welcome

Welcome Message
Ingrid Verbauwhede, UCLA, General Co-Chair

Symposium Highlights
Rajiv Joshi, IBM, TPC Co-Chair

9:00-10:30 Plenary Speech

Session Chair: Kiyoung Choi, SNU, TPC Co-Chair

I. *Low Power Requirements for Future Digital Life Style*
Ki Won Lee, Samsung

II. *Evolution of Low Power Electronics and Its Future Applications*
Tsugio Makimoto, Sony, Yoshio Sakai, Sony

10:30-10:50 Coffee Break

10:50-12:05 Session 1: Low Power Caches

Session Chair: Stephen Tang, Intel Corp.
Session Organizer: Tadahiro Kuroda, Keio Univ.

1.1s A Forward Body-Biased Low-Leakage SRAM Cache: Device and Architecture Considerations
Chris H. Kim, Purdue Univ., Jae-Joon Kim, Saibal Mukhopadhyay, Kaushik Roy

1.2s Reducing Translation Lookaside Buffer Active Power
Lawrence T. Clark, Intel Corp., Byungwoo Choi, Michael Wilkerson

1.3s A Power-Aware SWDR Cell for Reducing Cache Write Power
Yen-Jen Chang, NTU, Chia-Lin Yang, Feipei Lai

1.4s A Noise Tolerant Cache Design to Reduce Gate and Sub-threshold Leakage in the Nanometer Regime
Amit Agarwal, Purdue Univ., Kaushik Roy

1.5s Understanding and Minimizing Ground Bounce During Mode Transition of Power Gating Structures
Suhwan Kim, IBM, Stephen V. Kosonocky, Daniel R. Knebel

10:50-12:05 Session 2: Power Modeling and Optimization for Embedded Systems

Session Chair: Naehyuck Chang, SNU
Session Organizer: Diana Marculescu, CMU

2.1s Energy-Efficient Data Scrambling on Memory-Processor Interfaces
Luca Benini, Angelo Galati, Alberto Macii, Enrico Macii, Politecnico di Torino, Massimo Poncino

2.2s Analyzing the Energy Consumption of Security Protocols
Nachiketh R. Potlapally, Princeton Univ., Srivaths Ravi, Anand Raghunathan, Niraj K. Jha

2.3s LPBP: Low-Power Basis Profile of the Java 2 Micro Edition
Inseok Choi, Hyung Soo Kim, Heonshik Shin, Naehyuck Chang, SNU

2.4s Estimating Influence of Data Layout Optimizations on SDRAM Energy Consumption
Hyun Suk Kim, PSU, N. Vijaykrishnan, Mahmut Kandemir, Erik Brockmeyer, Francky Catthoor, Mary Jane Irwin

2.5s Analysis of Discharge Techniques for Multiple Battery Systems
Ravishankar Rao, Sarma Vrudhula, Univ. of Arizona, Daler Rakhmatov

12:05-13:30 Lunch

13:30-15:05 Session 3: Design Strategies for Active Power Reduction

Session Chair: Vivek De, Intel Corp.
Session Organizer: David Scott, Texas Instruments

3.1 A 225 MHz Resonant Clocked ASIC Chip
Conrad H. Ziesler, Univ. of Michigan, Joohee Kim, Visvesh S. Sathe, Marios C. Papaefthymiou

3.2 Energy Recovery Clocking Scheme and Flip-Flops for Ultra Low-Energy Applications
Matthew Cooke, Purdue Univ., Hamid Mahmoodi-Meimand, Kaushik Roy

3.3s A Semi-Custom Voltage-Island Technique and Its Application to High-Speed Serial Links
Juan Antonio Carballo, IBM, Jeffrey L. Burns, Seung-Moon Yoo, Ivan Vo, V. Robert Norman

3.4s Row-by-Row Dynamic Source-Line Voltage Control (RRDSV) Scheme for Two Orders of Magnitude Leakage Current Reduction of Sub-1-V-V_{DD} SRAM's
Kyeong-Sik Min, Kookmin Univ., Kouichi Kanda,Takayasu Sakurai

3.5s UDSM (Ultra-Deep Sub-Micron)-Aware Post-Layout Power Optimization for Ultra-Low Power CMOS VLSI
Kyu-won Choi, Georgia Tech., Abhijit Chatterjee

13:30-15:05 Session 4: Leakage Estimation

Session Chair: Farid Najm, Univ. of Toronto
Session Organizer: Yun Cao, Kyushu University

4.1 Full Chip Leakage Estimation Considering Power Supply and Temperature Variations
Haihua Su, IBM, Frank Liu, Anirudh Devgan, Emrah Acar, Sani Nassif

4.2 Statistical Estimation of Leakage Current Considering Inter- and Intra-Die Process Variation
Rajeev Rao, Univ. of Michigan, Ashish Srivastava, David Blaauw, Dennis Sylvester

4.3s Leakage Power Modeling and Optimization in Interconnection Networks
Xuning Chen, Princeton Univ., Li-Shiuan Peh

4.4s Leakage and Leakage Sensitivity Computation for Combinational Circuits
Emrah Acar, IBM, Anirudh Devgan, Rahul Rao, Ying Liu, Haigua Su, Sani Nassif, Jeffrey Burns

4.5s Efficient Techniques for Gate Leakage Estimation
Rahul M. Rao, Univ. of Michigan, Jeffrey L. Burns, Anirudh Devgan, Richard B. Brown

15:05-15:25 Coffee Break

15:25-17:00 Session 5: Design Strategies for Controlling Standby Leakage

Session Chair: Deog-Kyoon Jeong, SNU
Session Organizer: Ali Keshavarzi, Intel Corp.

5.1 Design Methodology for Fine-Grained Leakage Control in MTCMOS
Benton H. Calhoun, MIT, Frank A. Honore, Anantha Chandrakasan

5.2 An MTCMOS Design Methodology and Its Application to Mobile Computing
Hyo-Sig Won, Samsung, Kyo-Sun Kim, Kwang-Ok Jeong, Ki-Tae Park, Kyu-Myung Choi, Jeong-Taek Kong

5.3s Optimal Body Bias Selection for Leakage Improvement and Process Compensation Over Different Technology Generations
Cassondra Neau, Purdue Univ., Kaushik Roy

5.4s Effectiveness and Scaling Trends of Leakage Control Techniques for Sub-130nm CMOS Technologies
Bhaskar Chatterjee, University of Waterloo, Manoj Sachdev, Steven Hsu, Ram Krishnamurthy, Shekhar Borkar

5.5s An ASIC Design Methodology with Predictably Low Leakage, using Leakage-immune Standard Cells
Nikhil Jayakumar, Sunil P Khatr, Univ. of Colorado

15:25-17:00 Session 6: Advances in Low Power Synthesis

Session Chair: Steve Kang, UC Santa Cruz
Session Organizer: Massimo Poncino, Universita' di Verona

6.1 Low-Power High-Level Synthesis for FPGA Architectures
Deming Chen, UCLA, Jason Cong, Yiping Fan

6.2 ILP-Based Optimization of Sequential Circuits for Low Power
Feng Gao, Univ. of Michigan, John P. Hayes

6.3s Simultaneous Vt Selection and Assignment for Leakage Optimization
Ankur Srivastava, Univ. of Maryland

6.4s Effective Graph Theoretic Techniques for the Generalized Low Power Binding Problem
Azadeh Davoodi, Univ. of Maryland, Ankur Srivastava, Univ. of Maryland

6.5s Minimization of Dynamic and Static Power Through Joint Assignment of Threshold Voltages and Sizing Optimization
David Nguyen, UC Berkeley, Abhijit Davare, Michael Orshansky, David Chinnery, Brandon Thompson, Kurt Keutzer

17:00-17:20 Break

17:20-18:35 Session 7: Power Estimation and Design for Scaled Technologies
Session Chair: Wim Dehaene, KULeuven
Session Organizer: Takayasu Sakurai, University of Tokyo

7.1s Level Conversion for Dual-Supply Systems
Fujio Ishihara, Farhana Sheikh, Borivoje Nikolic, UC Berkeley

7.2s New Optimal Design Strategies and Analysis of Ultra-Low Leakage Circuits for Nano-Scale SOI Technology
Koushik K. Das, Univ. of Michigan, Rajiv V. Joshi, IBM, Ching-Te Chuang, Peter W. Cook, Richard B. Brown

7.3s Modeling and Estimation of Total Leakage Current in Nano-scaled CMOS Devices Considering the Effect of Parameter Variation
Saibal Mukhopadhyay, Purdue Univ., Kaushik Roy

7.4s A Clock Delayed Sleep Mode Domino Logic for Wide Dynamic OR Gate
Kwang-Il Oh, KAIST, Lee-Sup Kim

7.5s Strained-Si Devices and Circuits for Low-Power Applications
Keunwoo Kim, IBM, Rajiv V. Joshi, Ching-Te Chuang

17:20-18:30 Session 8: Low Power Analog Building Blocks
Session Chair: Byung-Gook Park, SNU
Session Organizer: Futao Yamaguchi, Sony

8.1s Low Power Startup Circuits for Voltage and Current Reference with Zero Steady State Current
Qadeer Ahmad Khan, Motorola, Sanjay Kumar Wadhwa, Motorola, Kulbhusan Misri

8.2s Reverse-Order Source/Drain Formation with Double Offset Spacer (RODOS) for CMOS Low-Power, High Speed and Low Noise Amplifiers
Woo Young Choi, SNU, Jong Duk Lee, Byung-Gook Park

8.3s Electric-Energy Generation Using Variable- Capacitive Resonator for Power-Free LSI: Efficiency Analysis and Fundamental Experiment
Masayuki Miyazaki, Hitachi, Hidetoshi Tanaka, Goichi Ono, Tomohiro Nagano, Norio Ohkubo, Takayuki Kawahara, Kazuo Yano

8.4 Temperature and Process Invariant MOS-Based Reference Current Generation Circuits for Sub-1V Operation
Stephen Tang, Intel Corp., Siva Narendra, Vivek De

19:15-21:00 Reception

TUESDAY, August 26, 2003

7:00-9:00 Breakfast

9:00-9:50 Keynote Speech 1
Session Chair: Kiyoung Choi, SNU, TPC Co-Chair

Title: Elements of Low Power Design for Integrated Systems
Sung-Mo (Steve) Kang, UCSC

9:50-10:10 Coffee Break

10:10-11:50 Session 9: Temperature and Power Aware Architectures
Session Chair: Trevor Mudge, Univ. of Michigan
Session Organizer: Srimat T. Chakradhar, NEC Laboratories

9.1 Microarchitecture Level Power and Thermal Simulation Considering Temperature Dependent Leakage Model
Weiping Liao, UCLA, Fei Li, Lei He

9.2s Reducing Power Density through Activity Migration
Seongmoo Heo, MIT, Kenneth Barr, Krste Asanovic

9.3s Pipeline Muffling and A Priori Current Ramping: Architectural Techniques to Reduce High-Frequency Inductive Noise
Michael D. Powell, T. N. Vijaykumar, Purdue Univ.

9.4s Integrated Architectural/Physical Planning Approach for Minimization of Current Surge in High Performance Clock-gated Microprocessors
Yiran Chen, Purdue Univ., Kaushik Roy, Cheng-Kok Koh

9.5s Reducing Reorder Buffer Complexity Through Selective Operand Caching
Gurhan Kucuk, Dmitry Ponomarev, State Univ. of New York, Oguz Ergin, Kanad Ghose

9.6s Routine based OS-aware Microprocessor Resource Adaptation for Run-time Operating System Power Saving
Tao Li, Univ. of Texas at Austin, Lizy Kurian John

10:10-11:50 Session 10: Design Contest Presentation
Session Chair: David Scott, TI
Session Organizer: Diana Marculescu, CMU

10.1 A 1.9GHz RF Transmit Beacon Using Environmentally Scavenged Energy Luminance Scaling
Shad Roundy, Brian P. Otis, Yuen-Hui Chee, Jan M. Rabaey, Paul Wright, UC Berkeley

10.2 Asynchronous Datapath with Software-controlled Adaptive Voltage Scaling
Yee William Li, George Patounakis, Kenneth L Shepard, Columbia Univ.

10.3 The ZebraNet Hardware Design
Pei Zhang, Margaret Martonosi, Princeton Univ.

10.4 A Compressed Frame Buffer to Reduce Display Power Consumption in Mobile Systems
Hojun Shim, Naehyuck Chang , SNU, Massoud Pedram, USC

10.5 Low Power Fully Parallel Content-Addressable Memory Based on Psuedo-CMOS Logic Structure
Chi-Sheng Lin, Kuan-Hua Chen, and Bin-Da Liu, National Cheng Kung Univ.

10.6 B#: A Battery Emulator and Power Profiling Instrument
Chulsung Park, Jinfeng Liu, and Pai H. Chou, UC Irvine

11:50-13:20 Lunch

13:20-14:10 Keynote Speech 2
Session Chair: Ingrid Verbauwhede, UCLA, General Co-Chair

Title: Ambient Intelligence – Industrial Research on a Visionary Concept
Werner Weber, Infineon

14:10-14:30 Coffee Break

14:30-16:00 Session 11: Power Efficient Cache Design
Session Chair: Wei Hwang, NCTU
Session Organizer: Shin-Dug Kim, Yonsei Univ.

11.1s Reducing Data Cache Energy Consumption via Cached Load/Store Queue
Dan Nicolaescu, UC Irvine, Alex Veidenbaum, Alex Nicolau

11.2s On Load Latency in Low-Power Caches
Soontae Kim, PSU, N. Vijaykrishnan, M. J. Irwin, L. K. John

11.3s Reducing Energy and Delay Using Efficient Victim Caches
Gokhan Memik, UCLA, Glenn Reinman, William H. Mangione-Smith

11.4s Low Cost Instruction Cache Designs for Tag Comparison Elimination
Youtao Zhang, Univ. of Texas at Dallas, Jun Yang

11.5s Lightweight Set Buffer: Low Power Data Cache for Multimedia Application
Jun Yang, UC Riverside, Jia Yu, Youtao Zhang

11.6s Non Redundant Data Cache
Carlos Molina, Universitat Rovira i Virgili, Carles Aliagas, Montse Garcia, Antonio Gonzalez, Jordi Tubella

14:30-16:00 Session 12: System Estimation and Voltage Scheduling
Session Chair: Wolfgang Nebel, Carl v. Ossietzky Univ.

Session Organizer: Kimiyoshi Usami, Shibaura Institute of Technology

12.1s A Critical Analysis of Application-Adaptive Multiple Clock Processors
Emil Talpes, Carnegie Mellon Univ., Diana Marculescu

12.2s Microprocessor Pipeline Energy Analysis
Karthik Natarajan, Univ. of Texas at Austin, Heather Hanson, Stephen W. Keckler, Charles R. Moore, Doug Burger

12.3s B#: a Battery Emulator and Power Profiling Instrument
Pai H. Chou, UC Irvine, Chulsung Park, Jae Park, Kien Pham, Jinfeng Liu

12.4s ESTIMA: An Architectural-Level Power Estimator for Multi-Ported Pipelined Register Files
Kavel M. Buyuksahin, Intel Corp., Priyadarsan Patra, Farid N. Najm

12.5s Multivoltage Scheduling with Voltage-Partitioned Variable Storage
Amitabh Menon, Texas Instruments, S.K.Nandy, Mahesh Mehendale

12.6s Voltage Scheduling Under Unpredictabilities: A Risk Management Paradigm
A. Davoodi, Ankur Srivastava, Univ. of Maryland

16:00-16:20 Break

16:20-17:50 Session 13: Energy Efficient Microarchitectural Techniques
Session Chair: Alice Wang, MIT
Session Organizer: Vojin Oklobdzija, UC Davis

13.1s Energy Efficient D-TLB and Data Cache using Semantic-Aware Multilateral Partitioning
Hsien-Hsin S. Lee, Chinnakrishnan S. Ballapuram, Georgia Tech.

13.2s A Selective Filter-Bank TLB System
Jung-Hoon Lee, Yonsei Univ., Gi-Ho Park, Sung-Bae Park, Shin-Dug Kim

13.3s Checkpointing Alternatives for High Performance, Power-Aware Processors
Andreas Moshovos, Univ. of Toronto

13.4s Reducing Instruction Fetch Energy with Backwards Branch Control Information and Buffering
Jude A. Rivers, IBM, Sameh Asaad, John-David Wellman, Jaime H. Moreno

13.5s Pipeline Stage Unification: A Low-Energy Consumption Technique for Future Mobile Processors
Hajime Shimada, Nagoya Univ., Hideki Ando, Toshio Shimada

13.6s Energy-Efficient Instruction Set Synthesis for Application-Specific Processors
Jong-eun Lee, SNU, Kiyoung Choi, SNU, Nikil D. Dutt, UC Irvine

16:20-17:45 Session 14: High Speed Converters, Amplifiers, and Low Power Analog Circuits
Session Chair: Lucien Breems, Philips
Session Organizer: Hong-June Park, Postech

14.1s A Low-Power Design Methodology for High-Resolution Pipelined Analog-to-Digital Converters
Reza Lotfi, Univ. of Tehran, Mohammad Taherzadeh-Sani, M. Yaser Azizi, Omid Shoaei

14.2s A 1-V 1-mW High-Speed Class AB Operational Amplifier for High-Speed Low Power Pipelined A/D Converters using "Slew Boost" Technique
H.A. Aslanzadeh, Sharif Univ. of Technology, S.Mehrmanesh, M.B.Vahidfar, A.Q.Safarian, Reza Lotfi

14.3s Low-Voltage Low-Power and Fast-Settling CMOS Operational Transconductance Amplifiers for Switched-Capacitor Applications
Mohammad Yavari, Univ. of Tehran, Omid Shoaei

14.4s Low-Voltage Low-Power High dB-Linear CMOS Exponential Function Generator using Highly-Linear V-I Converter
Quoc-Hoang Duong, ICU, Trung-Kien Nguyen, Sang-Gug Lee

14.5 A New Architecture for Rail-to-Rail Input Constant-gm CMOS Operational Transconductance Amplifiers
Mohammad M Ahmadi, Reza Lotfi, Univ. of Tehran, Mehrdad Sharif-Bakhtiar

18:30-22:00 Banquet

WEDNESDAY, August 27, 2003

7:00-9:00 Breakfast

9:00-9:50 Keynote Speech 3
Session Chair: Rajiv Joshi, IBM, TPC Co-Chair

Title: *A Systems Approach to Molecular Electronics*
James R. Heath, Caltech

9:50-10:10 Coffee Break

10:10-11:50 Session 15: Circuit Considerations for Low Power
Session Chair: Chong-Min Kyung, KAIST
Session Organizer: Suhwan Kim, IBM T. J. Watson Research Center

15.1 Energy-Aware Architectures for a Real-Valued FFT Implementation
Alice Wang, MIT, Anantha P. Chandrakasan

15.2s A Low Power VLSI Architecture for Turbo Decoding
Seok-Jun Lee, Univ. of Illinois, Naresh R. Shanbhag, Andrew C. Singer

15.3s A Mixed-Clock Issue Queue Design for Globally Asynchronous, Locally Synchronous Processor Cores
Venkata Syam P. Rapaka, Carnegie Mellon Univ., Diana Marculescu

15.4s Power Efficient Comparators for Long Arguments in Superscalar Processors
Dmitry Ponomarev, State Univ. of New York, Gurhan Kucuk, Oguz Ergin, Kanad Ghose

15.5s The Microarchitecture of a Low Power Register File
Nam Sung Kim, Univ. of Michigan, Trevor Mudge

15.6s Branch Prediction on Demand : an Energy-Efficient Solution
Daniel Chaver, Universidad Complutense, Luis Pinuel, Manuel Prieto, Francisco Tirado, Michael C. Huang

10:10-11:50 Session 16: System Level Issues
Session Chair: Flavius Gruian, Lund Univ.
Session Organizer: Mani Srivastava, UCLA

16.1 Dynamic Voltage Scaling Algorithm for Fixed-Priority Real-Time Systems Using Work-Demand Analysis
Woonseok Kim, Jihong Kim, Sang Lyul Min, SNU

16.2s Exploiting Program Hotspots and Code Sequentiality for Instruction Cache Leakage Management
Jie S Hu, PSU, Avanti Nadgir, N. Vijaykrishnan, Mary Jane Irwin, Mahmut Kandemir

16.3s Power-Aware Scheduling of Conditional Task Graphs in Real-Time Multiprocessor Systems
Dongkun Shin, Jihong Kim, SNU

16.4s Exploiting Compiler-Generated Schedules for Energy Savings in High-Performance Processors
Madhavi Valluri, Univ. of Texas at Austin, Lizy John, Heather Hanson

16.5s Energy-Aware Memory Allocation in Heterogeneous Non-Volatile Memory Systems
Hyung Gyu Lee, Naehyuck Chang, SNU

16.6s Energy Characterization of a Tiled Architecture Processor with On-Chip Networks
Jason Sungtae Kim, Michael Bedford Taylor, Jason Miller, David Wentzlaff, MIT

11:50-13:20 Lunch

13:20-14:10 Keynote Speech 4
Session Chair: Rajiv Joshi, IBM, TPC Co-Chair

Title: Low Power RF IC Design for Wireless Communication
Domine M.W. Leenaerts, Philips

14:10-14:30 Break

14:30-16:05 Session 17: RF Communication Circuits
Session Chair: Domine Leenaerts, Philips
Session Organizer: Kevin Kornegay, IBM

17.1 A Power-Optimized Widely-Tunable 5-GHz Monolithic VCO in a Digital SOI CMOS Technology on High Resistivity Substrate
Jonghae Kim, IBM, Jean-Olivier Plouchart, IBM, Noah Zamdmer, Melanie Sherony, Yue Tan, Meeyoung Yoon, Robert Trzcinski, Mohamed Talbi, John Safran, Asit Ray, Lawrence Wagner

17.2s A 0.123 mW 7.25 GHz Static Frequency Divider by 8 in a 120-nm SOI Technology
Jean-Olivier Plouchart, IBM, Jonghae Kim, IBM, Hector Recoules, Noah Zamdmer, Yue Tan, Melanie Sherony, Asit Ray, Lawrence Wagner

17.3s A 0.75-mW Analog Processor IC for Wireless Biosignal Monitor

Chih-jen Yen, Chung-Yuan Christian Univ., Wen –Yaw Chung, Mely Chen Chi, Shing-Hao Lee

17.4 Integrated DC-DC Converter Design for Improved WCDMA Power Amplifier Efficiency in SiGe BiCMOS Technology
Drew Guckenberger, Cornell Univ., Kevin Kornegay

17.5s A Novel High Frequency, High-Efficiency, Differential Class-E Power Amplifier in 0.18um CMOS
Payam Heydari, UC Irvine, Ying Zhang

14:30-16:05 Session 18: Sensor Networks and Communication Systems
Session Chair: Sarma Vrudhula, Univ. of Arizona
Session Organizer: Youngsoo Shin, IBM T. J. Watson Research Center

18.1 Energy Optimization Techniques in Cluster Interconnects
Eun Jung Kim, PSU, Ki Hwan Yum, G. M. Link, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, M. Yousif, C. R. Das

18.2s Uncertainty-Based Scheduling: Energy-Efficient Ordering for Tasks with Variable Execution Time
Flavius Gruian, Lund Univ., Krzysztof Kuchcinski

18.3s Energy Efficiency and Fairness Tradeoffs in Multi-Resource, Multi-Tasking Embedded Systems
Sung I. Park, Vijay Raghunathan, UCLA, Mani B. Srivastava

18.4 Low Power Coordination in Wireless Ad-hoc Networks
Farinaz Koushanfar, UC Berkely, Abhijit Davare, David Tong Nguyen, Miodrag Potkonjak, Alberto Sangiovanni-Vincentelli

18.5s An Environmental Energy Harvesting Framework for Sensor Networks
Aman Kansal, UCLA, Mani B Srivastava

16:05-16:15 Closing Remarks
Ingrid Verbauwhede, UCLA, General Co-Chair
Rajiv Joshi, IBM, TPC Co-Chair